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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/615,938	07/13/2000	Kenji Shimazaki	32809	3985

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EXAMINER

BARAN, MARY C

ART UNIT PAPER NUMBER

2857

DATE MAILED: 08/14/2002

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Applicant(s)	SHIMAZAKI ET AL.	
	Application No.	09/615,938	
	Examiner	Art Unit	
	Mary Kate Baran	2857	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 13 July 2000.
- 2a) ☐ This action is FINAL. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-8 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1, 3 and 5-8 is/are rejected.
- 7) ☒ Claim(s) 2 and 4 is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☒ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on _____ is/are: a) ☐ accepted or b) ☒ objected to by the Examiner.
- Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
- 11) ☐ The proposed drawing correction filed on _____ is: a) ☐ approved b) ☐ disapproved by the Examiner.
- If approved, corrected drawings are required in reply to this Office action.
- 12) ☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

- 13) ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
 2. ☐ Certified copies of the priority documents have been received in Application No. _____.
 3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
- * See the attached detailed Office action for a list of the certified copies not received.
- 14) ☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).
- a) ☐ The translation of the foreign language provisional application has been received.
- 15) ☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

- | | |
|--|---|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892) | 4) <input type="checkbox"/> Interview Summary (PTO-413) Paper No(s). _____ |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152) |
| 3) <input checked="" type="checkbox"/> Information Disclosure Statement(s) (PTO-1449) Paper No(s) <u>3</u> . | 6) <input type="checkbox"/> Other: |

DETAILED ACTION

Drawings

1. The drawings are objected to because the labels have not been translated within the figures. While a separate labeled sheet supplying the translation has been provided, the examiner requests the translation be within the figures. A proposed drawing correction or corrected drawings are required in reply to the Office action to avoid abandonment of the application. The objection to the drawings will not be held in abeyance.

Specification

2. The lengthy specification has not been checked to the extent necessary to determine the presence of all possible minor errors. Applicant's cooperation is requested in correcting any errors of which applicant may become aware in the specification.

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

Claims 1 and 3 are rejected under 35 U.S.C. 103(a) as being unpatentable over Finman (U.S. Patent No. 5,117,377) in view of Hatsuda (U.S. Patent No. 6,066,177).

Referring to claim 1, Finman teaches analyzing electromagnetic interference which develops in an LSI (see Finman, col. 1 lines 7-12), comprising a correction step of correcting the amplitude of a signal in each node (see Finman, col. 5 lines 3-8), an addition step of adding the signals of all nodes together within a period of time corresponding to one cycle, provided that the thus-corrected signal appears at the time the signal arrives at the node (see Finman, col. 5 lines 8-14), and a frequency analysis step of analyzing the frequency of the signal, calculated in the addition step (see Finman, col. 6 lines 64-68). The examiner interprets the term "generic analyzer" as disclosed in Finman to mean the same as the claimed term "frequency analyzer" (see Finman, col. 12 lines 29-34). Finman does not teach generating a current waveform, and calculating the current, which has been prepared for each change in each node, in accordance with the probability of variation in each node.

Hatsuda teaches providing a current waveform for each path (see Hatsuda, Figure 17; S203, S204), and calculating the current in accordance with the probability of change in each node (see Hatsuda, col. 22 lines 8-12).

It would have been obvious at the time the invention was made to one of ordinary skill in the art to modify Finman to include the teachings of Hatsuda, because calculating the current based on the probability of change allows the system to anticipate the voltage change of the various paths, and this voltage information enables

a reliable current calculation (see Hatsuda, col. 21 line 59-col. 22 line 12 and col. 4 lines 65-67).

Referring to claim 3, as noted above Finman and Hatsuda teach all. Hatsuda further teaches each node having a plurality of signal transmission paths, and each of the current waveforms (see Hatsuda, Figure 17; S203, S204) is calculated in consideration of a case where each of the paths has a unique probability of change (see Hatsuda, col. 22 lines 8-12) and signal arrive time (see Hatsuda, Figure 17; S02, S201). It would have been obvious at the time the invention was made to one of ordinary skill in the art to modify Finman to include the teachings of Hatsuda, because calculating current with respect to circuit delay determines if the current is generated from either a rise or a fall delay and further enables an easy and analytical calculation of the current (see Hatsuda, col. 23 lines 10-28 and col. 4 lines 46-49).

4. Claims 5-8 are rejected under 35 U.S.C. 103(a) as being unpatentable over Tamaki et al. (U.S. Patent No. 5,784,285) in view of Hatsuda (U.S. Patent No. 6,066,177).

Referring to claims 5 and 7, Tamaki et al. teaches analyzing electromagnetic interference which develops in an LSI (see Tamaki et al., col. 1 lines 5-9), comprising a waveform formation step forming a current estimation waveform (see Tamaki et al., col. 2 line 42) which has been prepared for each change in each node as if the waveform randomly arises within a plurality of predetermined cycles (see Tamaki et al., col. 2 lines

43-48), adding the thus prepared current estimation waveforms of all nodes to thereby derive a current waveform (see Tamaki et al., col. 2 lines 49-52), and analyzing the frequency of the current waveform, thereby determining a noise characteristic of EMI (see Tamaki et al., col. 5 lines 1-7 and lines 16-20). Tamaki et al. does not teach calculating the current, which has been prepared for each change in each node, in accordance with the probability of change in each node and a time at which a signal arrives at each node.

Hatsuda teaches calculating the current in accordance with the probability of change in each node (see Hatsuda, col. 22 lines 8-12) and a time at which a signal arrives at each node (see Hatsuda, col. 23 lines 10-28).

It would have been obvious at the time the invention was made to one of ordinary skill in the art to modify Tamaki et al. to include the teachings of Hatsuda, because calculating the current based on the probability of change indicates voltage variation of the lines, which enables a reliable calculation of the saturation current (see Hatsuda, col. 21 line 59-col. 22 line 12 and col. 4 lines 65-67).

Referring to claims 6 and 8, as noted above Tamaki et al. and Hatsuda teach all. Hatsuda further discloses a method wherein each node has a plurality of paths and a current is calculated in consideration of a case where each of the paths has a unique probability of change (see Hatsuda, col. 22 lines 8-12) and signal arrival time (see Hatsuda, col. 23 lines 10-28). It would have been obvious at the time the invention was made to one of ordinary skill in the art to modify Finman to include the teachings of

Hatsuda, because calculating current with respect to circuit delay enables an easy and analytical calculation of the time with respect to the current (see Hatsuda, col. 23 lines 10-28 and col. 4 lines 46-49).

Allowable Subject Matter

5. Claims 2 and 4 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Conclusion

6. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Fishburn discloses a method and apparatus for calibrating a static timing analyzer to path delay measurements.

Calero discloses a process for producing time dependent waveforms of positive and negative symmetrical sequence components of a power system's voltages or currents.

Barbour et al. discloses a system for receiving and enhancing electromagnetic radiation input signals.

McKim, Jr., et al. discloses an AC test system for measuring current harmonics and voltage variations.


Art Unit: 2857

7. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Mary Kate Baran whose telephone number is (703) 305-4474. The examiner can normally be reached on Monday - Friday from 8:00 am to 5:00 pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Marc S Hoff can be reached on (703) 308-1677. The fax phone numbers for the organization where this application or proceeding is assigned are (703) 872-9318 for regular communications and (703) 872-9319 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 308-1782.

MCB
August 9, 2002


MARC S. HOFF
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2800